

# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

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- 3-State Q Outputs Drive Bus Lines Directly
- Counter Operation Independent of 3-State Output
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

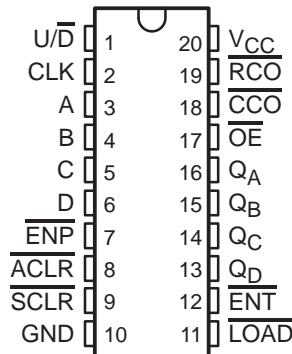
The SN74ALS568A decade counter and 'ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock (CLK) input.

The clear function is initiated by applying a low level to either asynchronous clear ( $\overline{\text{ACLR}}$ ) or synchronous clear ( $\overline{\text{SCLR}}$ ). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding load ( $\overline{\text{LOAD}}$ ) low during a positive-going clock transition. The counting function is enabled only when enable P ( $\overline{\text{ENP}}$ ) and enable T ( $\overline{\text{ENT}}$ ) are low and  $\overline{\text{ACLR}}$ ,  $\overline{\text{SCLR}}$ , and  $\overline{\text{LOAD}}$  are high. The up/down ( $\overline{\text{U/D}}$ ) input controls the direction of the count. These counters count up when  $\overline{\text{U/D}}$  is high and count down when  $\overline{\text{U/D}}$  is low.

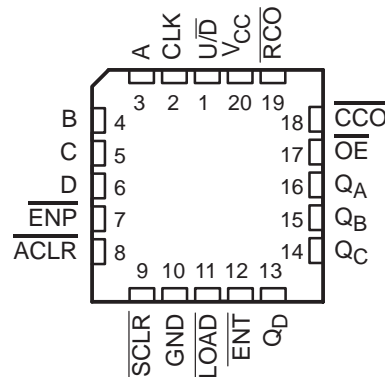
A high level at the output-enable ( $\overline{\text{OE}}$ ) input forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of  $\overline{\text{OE}}$ .  $\overline{\text{ENT}}$  is fed forward to enable the ripple-carry output ( $\overline{\text{RCO}}$ ) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The clocked carry output ( $\overline{\text{CCO}}$ ) produces a low-level pulse for a duration equal to that of the low level of the clock when  $\overline{\text{RCO}}$  is low and the counter is enabled (both  $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$  are low); otherwise,  $\overline{\text{CCO}}$  is high.  $\overline{\text{CCO}}$  does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting  $\overline{\text{RCO}}$  or  $\overline{\text{CCO}}$  of the first counter to  $\overline{\text{ENT}}$  of the next counter. However, for very high-speed counting,  $\overline{\text{RCO}}$  should be used for cascading since  $\overline{\text{CCO}}$  does not become active until the clock returns to the low level.

The SN54ALS569A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS568A and SN74ALS569A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS569A . . . J PACKAGE  
SN74ALS568A, SN74ALS569A . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS569A . . . FK PACKAGE  
(TOP VIEW)



**SN54ALS569A, SN74ALS568A, SN74ALS569A**  
**SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS**  
**WITH 3-STATE OUTPUTS**

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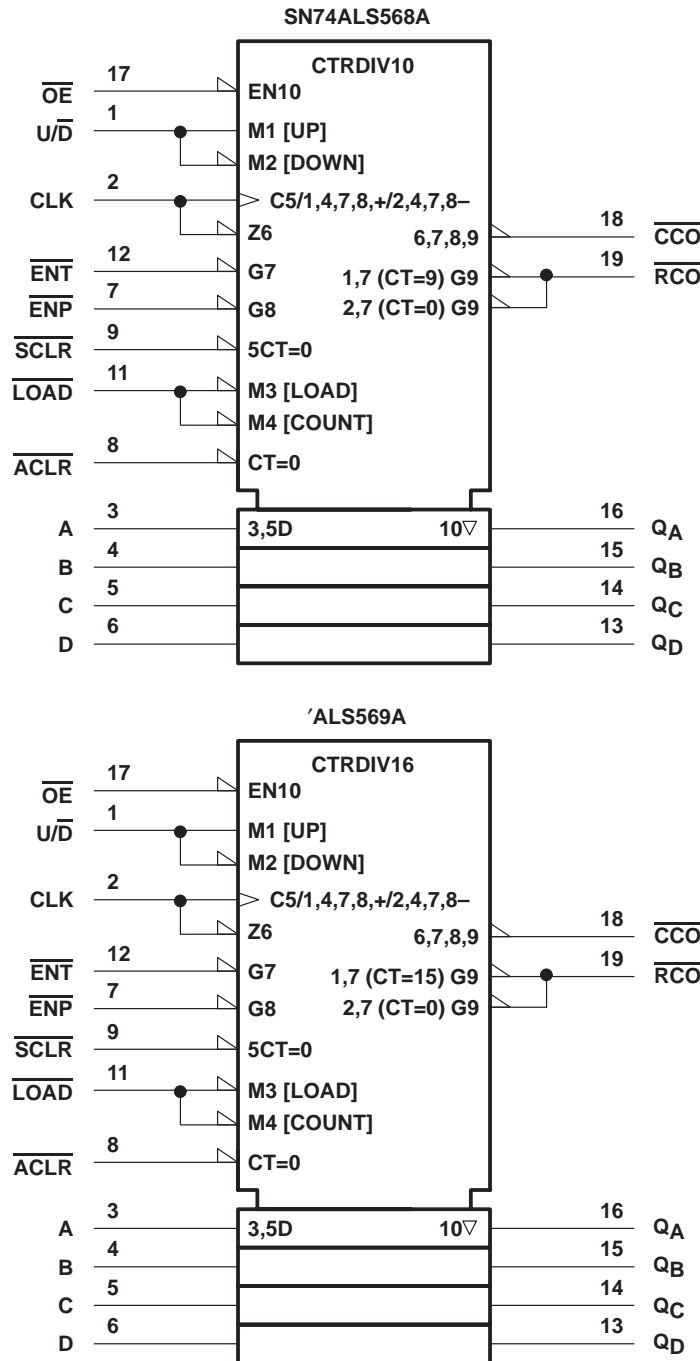
FUNCTION TABLE

INPUTS								OPERATION
$\overline{OE}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/D	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	↑	Synchronous clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count up
L	H	H	H	L	L	L	↑	Count down
L	H	H	H	H	X	X	X	Inhibit count
L	H	H	H	X	H	X	X	Inhibit count

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logic symbols†

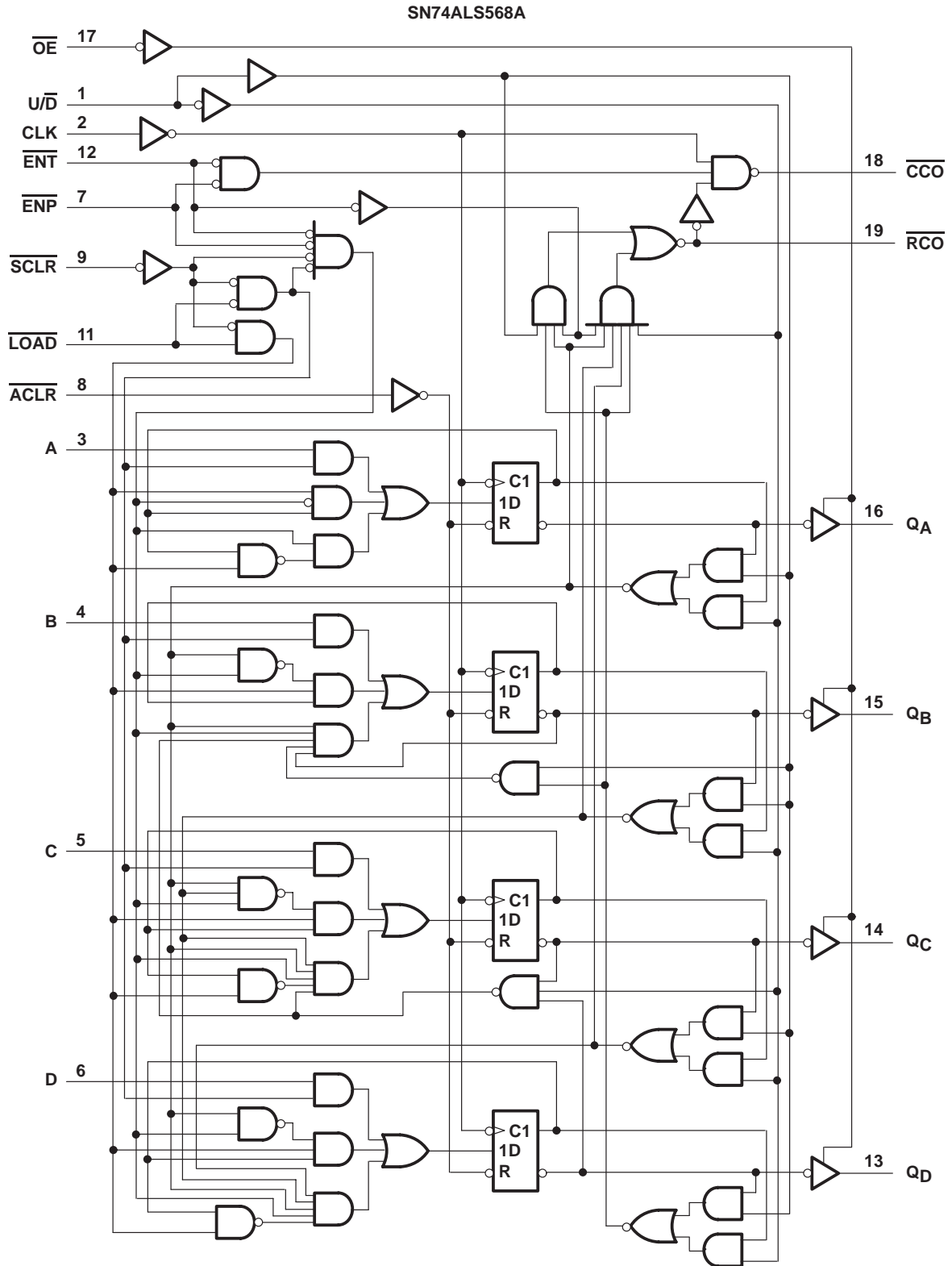


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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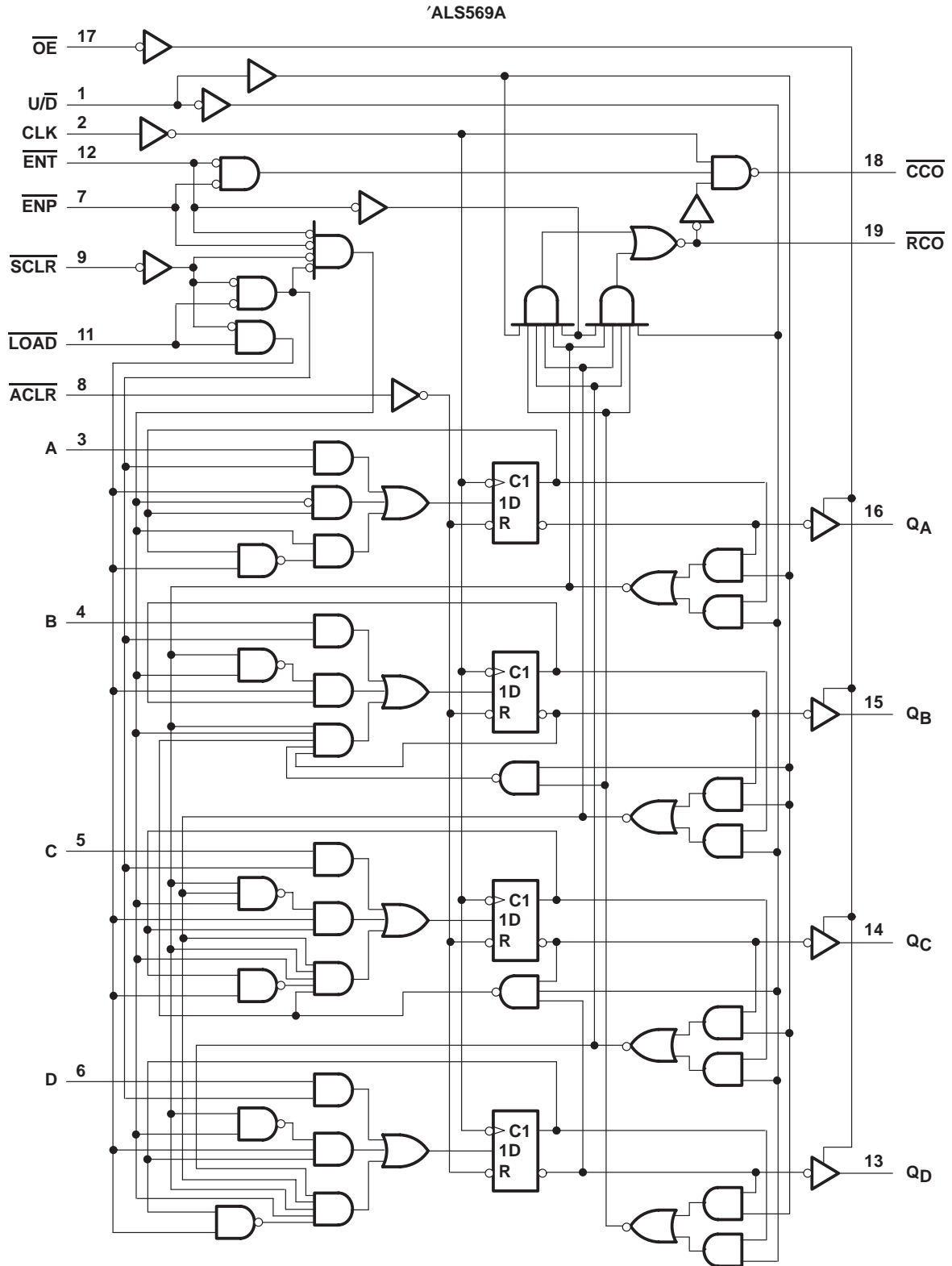
## logic diagrams (positive logic)



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

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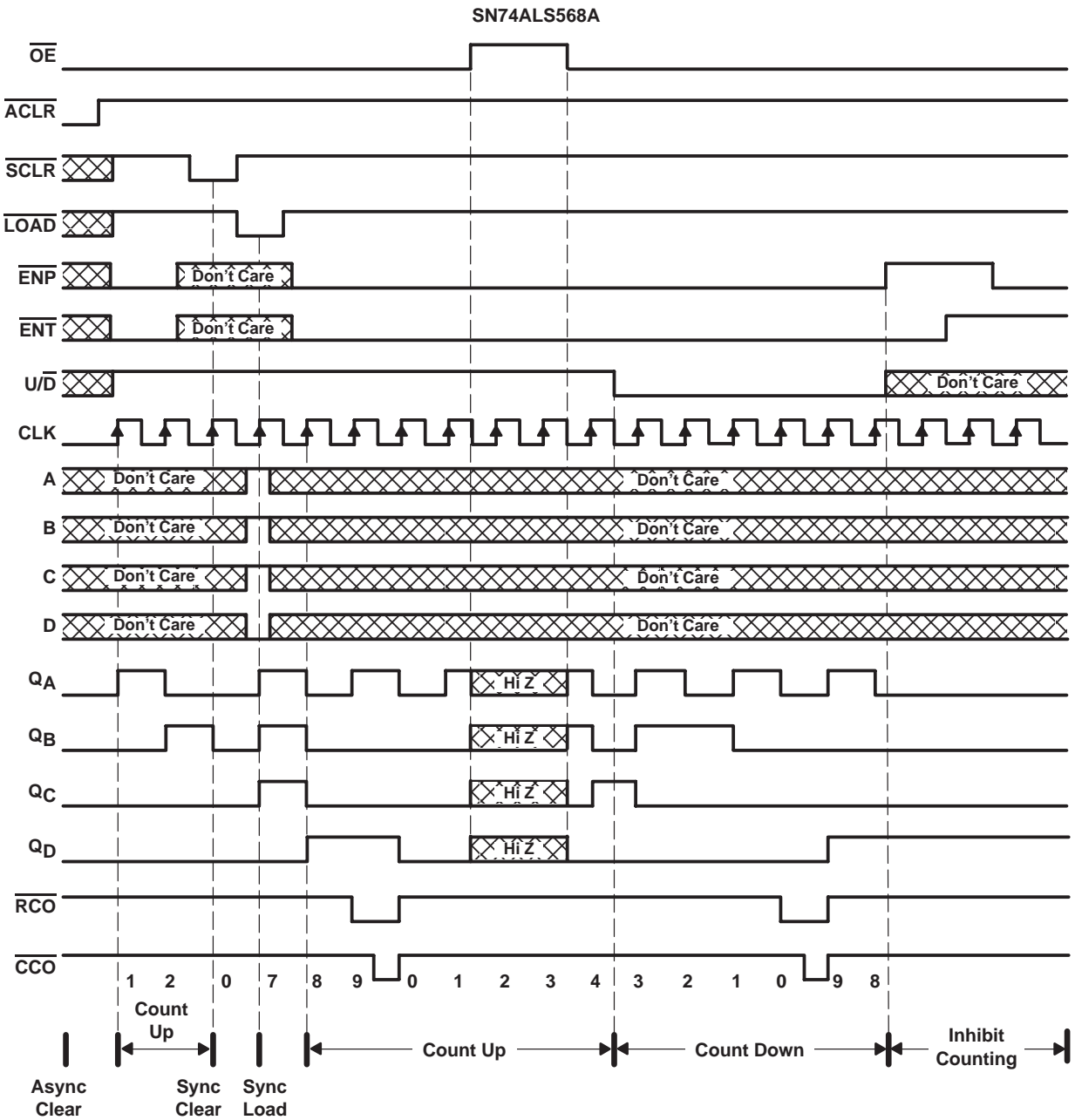
## logic diagrams (positive logic) (continued)



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

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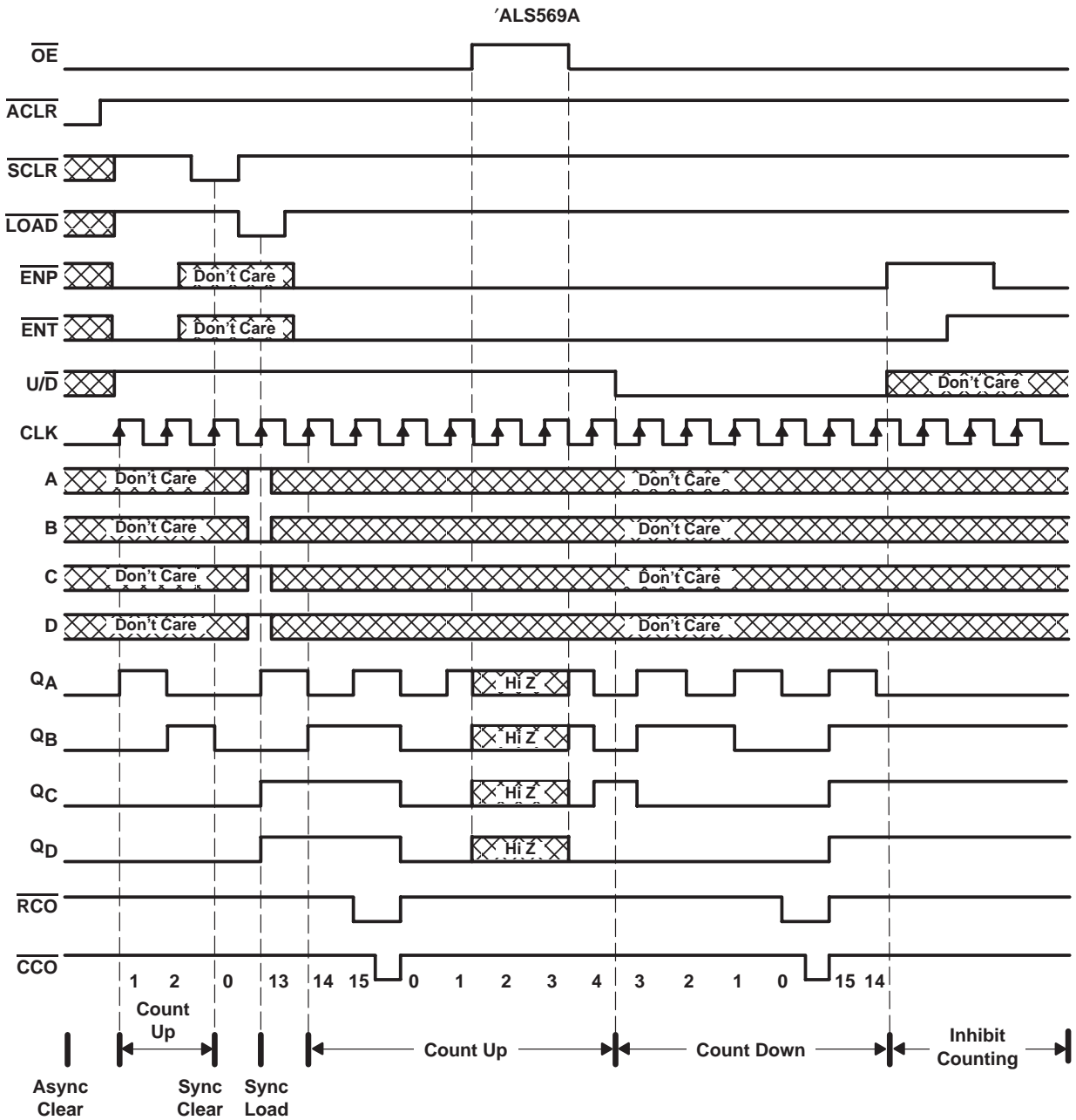
## typical load, count, and inhibit sequences



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

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## typical load, count, and inhibit sequences (continued)



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS569A	–55°C to 125°C
SN74ALS568A, SN74ALS569A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current	Q outputs		–1	–2.6		mA	
		$\overline{CCO}$ and $\overline{RCO}$		–0.4	–0.4			
$I_{OL}$	Low-level output current	Q outputs		12	24		mA	
		$\overline{CCO}$ and $\overline{RCO}$		4	8			
$f_{clock}$	Clock frequency	SN74ALS568A			0	20	MHz	
		'ALS569A		0	22	30		
$t_w$	Pulse duration	$\overline{ACLR}$ or $\overline{LOAD}$ low		20	15		ns	
		SN74ALS568A	CLK high		25			
			CLK low		25			
		'ALS569A	CLK high	20	16.5			
CLK low	23		16.5					
$t_{su}$	Setup time before $CLK\uparrow$	Data at A, B, C, D		25	20		ns	
		$\overline{ENP}$ , $\overline{ENT}$	High	35	30			
			Low	25	20			
		$\overline{SCLR}$	Low	20	15			
			High (inactive)	35	30			
		$\overline{LOAD}$	Low	20	15			
			High (inactive)	35	30			
$\overline{U/D}$		35	30					
$\overline{ACLR}$ inactive		10	10					
$t_h$	Hold time after $CLK\uparrow$ for any input	0			0		ns	
$T_A$	Operating free-air temperature	–55		125	0	70	°C	





# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.5			-1.5			V	
$V_{OH}$	All outputs	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V	
	Q outputs	$V_{CC} = 4.5\text{ V}$		2.4 3.3							
$V_{OL}$	Q outputs	$V_{CC} = 4.5\text{ V}$		0.25 0.4			0.25 0.4			V	
				0.35 0.5							
	$\overline{CCO}$ and $\overline{RCO}$		$V_{CC} = 4.5\text{ V}$		0.25 0.4			0.25 0.4			
					0.35 0.5						
$I_{OZH}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$		20			20			$\mu\text{A}$	
$I_{OZL}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$		-20			-20			$\mu\text{A}$	
$I_I$		$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$		0.1			0.1			mA	
$I_{IH}$		$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$		20			20			$\mu\text{A}$	
$I_{IL}$		$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$		-0.2			-0.2			mA	
$I_{O\ddagger}$	$\overline{CCO}$ and $\overline{RCO}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$		-15 -70			-15 -70			mA	
	Q outputs			-20 -112			-30 -112				
$I_{CC}$	$V_{CC} = 5.5\text{ V}$		Outputs high	16 26			16 26			mA	
			Outputs low	20 32			20 32				
			Outputs disabled	20 32			20 32				

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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## switching characteristics (see Figure 1)

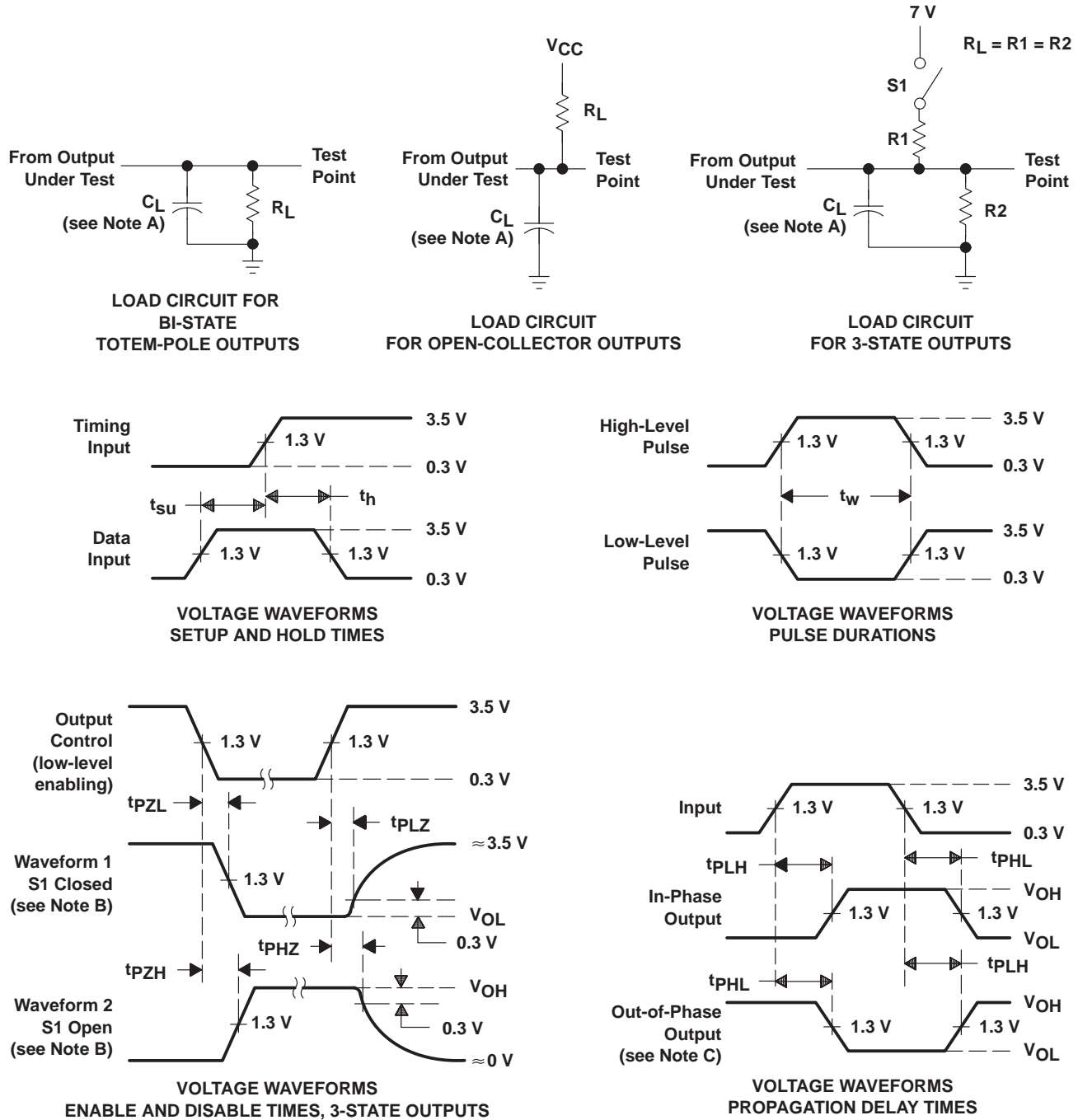
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS569A		SN74ALS568A SN74ALS569A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>	SN74ALS568A				20	MHz	
	'ALS569A		22	30			
t <sub>PLH</sub>	CLK	Any Q	4	21	4	13	ns
t <sub>PHL</sub>			7	19	7	16	
t <sub>PLH</sub>	CLK	$\overline{RCO}$	12	37	12	28	ns
t <sub>PHL</sub>			10	28	10	19	
t <sub>PLH</sub>	CLK	$\overline{CCO}$	5	17	5	13	ns
t <sub>PHL</sub>			6	30	6	25	
t <sub>PLH</sub>	U/ $\overline{D}$	$\overline{RCO}$	9	31	9	23	ns
t <sub>PHL</sub>			9	33	9	19	
t <sub>PLH</sub>	$\overline{ENT}$	$\overline{RCO}$	6	21	6	15	ns
t <sub>PHL</sub>			4	20	4	13	
t <sub>PLH</sub>	$\overline{ENT}$	$\overline{CCO}$	5	18	5	13	ns
t <sub>PHL</sub>			9	32	9	23	
t <sub>PLH</sub>	$\overline{ENP}$	$\overline{CCO}$	4	18	4	12	ns
t <sub>PHL</sub>			5	18	5	14	
t <sub>PHL</sub>	$\overline{ACLR}$	Any Q	9	25	9	20	ns
t <sub>PZH</sub>	$\overline{OE}$	Any Q	6	23	6	18	ns
t <sub>PZL</sub>			6	29	6	24	
t <sub>PHZ</sub>	$\overline{OE}$	Any Q	1	12	1	10	ns
t <sub>PLZ</sub>			3	29	3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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