

# CD40194B Types

## CMOS 4-Bit Bidirectional Universal Shift Register

High-Voltage Types (20 Volt Rating)

■ CD40194B is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the RESET input resets all stages and forces all outputs low.

The CD40194B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix). The CD40194B is similar to industry types 340194 and MC40194.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

<b>DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)</b>	
Voltages referenced to V <sub>SS</sub> Terminal	-0.5V to +20V
<b>INPUT VOLTAGE RANGE, ALL INPUTS</b>	-0.5V to V <sub>DD</sub> +0.5V
<b>DC INPUT CURRENT, ANY ONE INPUT</b>	±10mA
<b>POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):</b>	
For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
<b>DEVICE DISSIPATION PER OUTPUT TRANSISTOR</b>	
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
<b>OPERATING-TEMPERATURE RANGE (T<sub>A</sub>)</b>	-55°C to +125°C
<b>STORAGE TEMPERATURE RANGE (T<sub>stg</sub>)</b>	-65°C to +150°C
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

**NOT RECOMMENDED FOR NEW DESIGNS**

**Features:**

- Medium-speed: f<sub>CL</sub> = 12 MHz (typ.) @ V<sub>DD</sub> = 10 V
- Fully static operation
- Synchronous parallel or serial operation
- Asynchronous master reset
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

**Applications:**

- Arithmetic unit bus registers
- Serial/parallel conversions
- General-purpose register for bus-organized systems
- General-purpose registers

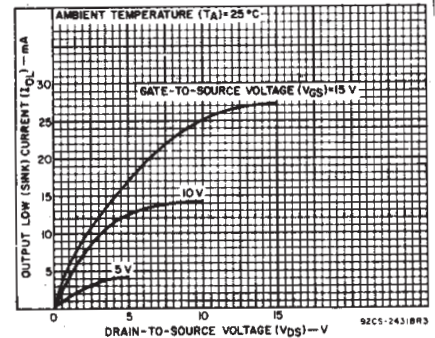
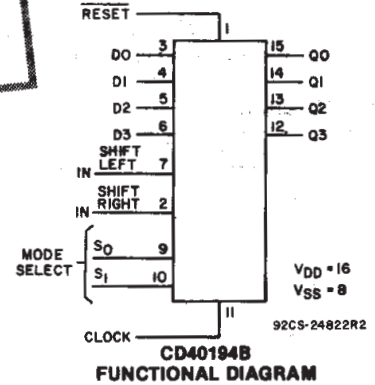


Fig. 1—Typical n-channel output low (sink) current characteristics.

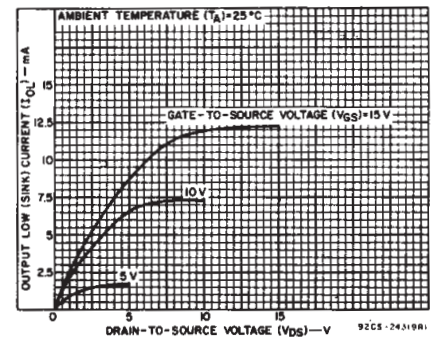


Fig. 2—Minimum n-channel output low (sink) current characteristics.




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**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ , Except as Noted.  
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For Package-Temperature Range)		3	18	V
Setup Time, D0, D3, SR <sub>IN</sub> , SL <sub>IN</sub> to clock	5	100	—	ns
	10	70	—	
	15	50	—	
SELECT 0, SELECT 1 to clock	5	400	—	
	10	220	—	
	15	130	—	
Hold Time, D0, D03, SR <sub>IN</sub> , SL <sub>IN</sub> to clock	5	0	—	
	10	0	—	
	15	0	—	
SELECT 0, SELECT 1 to clock	5	0	—	
	10	0	—	
	15	0	—	
Clock Pulse Width,	5	180	—	
	10	80	—	
	15	50	—	
Clock Input Frequency	5	—	3	MHz
	10	—	6	
	15	—	8	
Clock Input Rise or Fall Time,	5	1000	—	μs
	10	100	—	
	15	100	—	
Reset Pulse Width,	5	300	—	ns
	10	200	—	
	15	140	—	

### CONTROL TRUTH TABLE FOR CD40194B SERIES

CLOCK	MODE SELECT		RESET	ACTION
	S <sub>0</sub>	S <sub>1</sub>		
X	0	0	1	No Change
	1	0	1	Shift Right (Q0 toward Q3)
	0	1	1	Shift Left (Q3 toward Q0)
	1	1	1	Parallel Load
X	X	X	0	Reset

1 = High level  
 0 = Low level

X = Don't care  
 ▲ = Level change

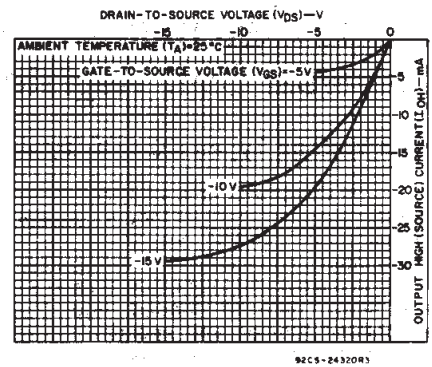


Fig. 3—Typical p-channel output high (source) current characteristics.

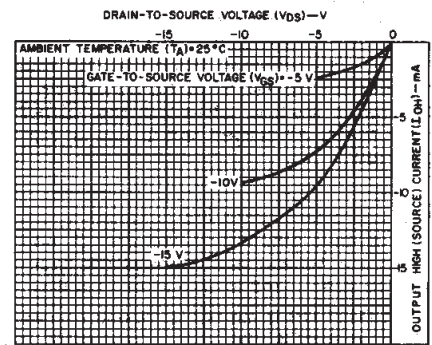


Fig. 4—Minimum p-channel output high (source) current characteristics.

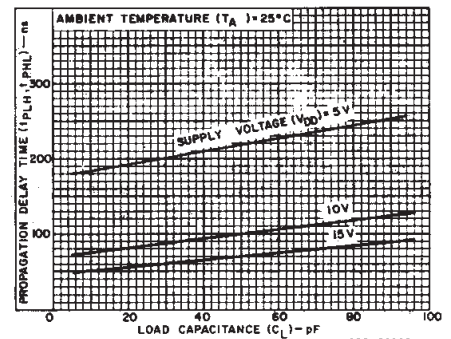


Fig. 5—Typical propagation delay time as a function of load capacitance, (CLOCK to Q).

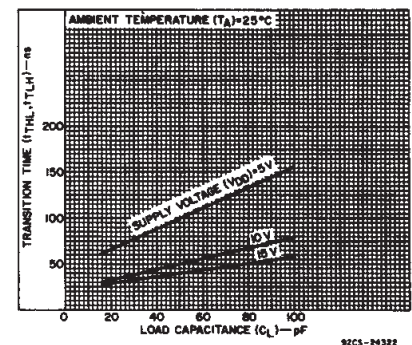


Fig. 6—Typical transition time as a function of load capacitance.

# CD40194B Types

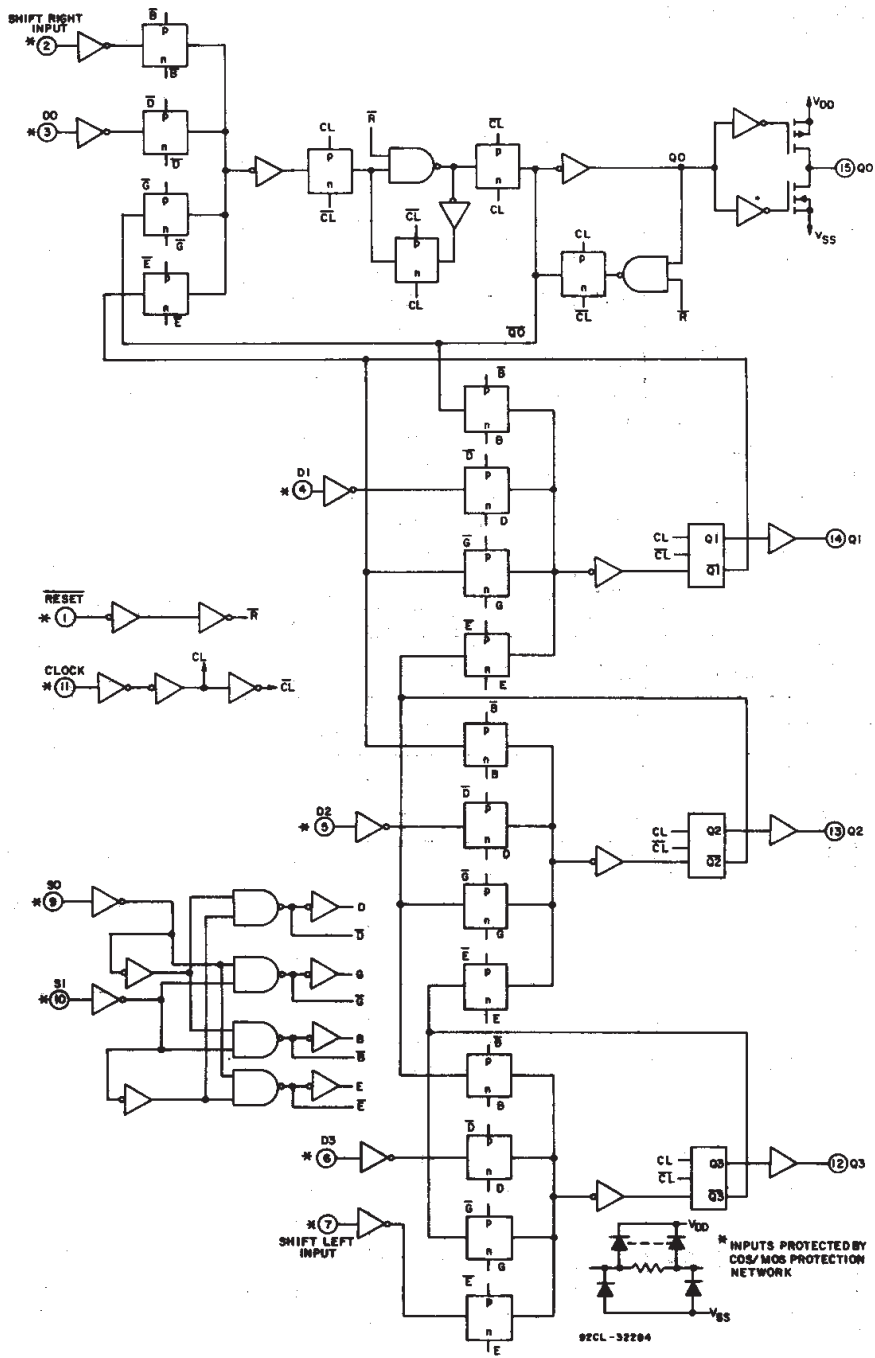


Fig. 8—CD40194B logic diagram.

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## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.8	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA
3-State Output Leakage Current, I <sub>OUT</sub> Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 <sup>-4</sup>	±0.4	μA

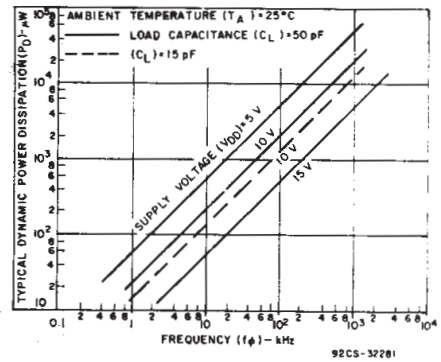


Fig. 9—Typical power dissipation as a function of frequency.

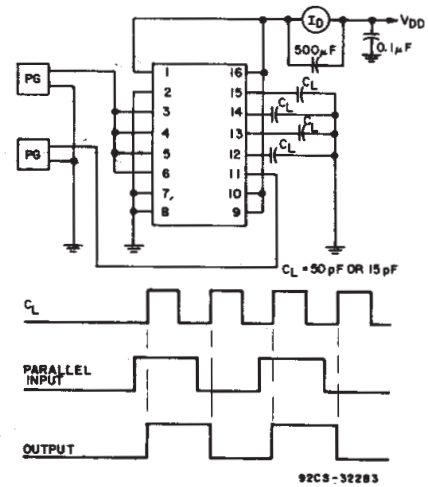


Fig. 10—Dynamic power dissipation test circuit.

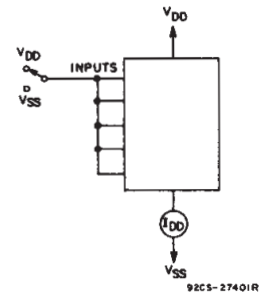


Fig. 11—Quiescent device current test circuit.

# CD40194B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  
 Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS		
		VDD V	Min.	Typ.		Max.	
Propagation Delay Time: Clock to Q $t_{PHL}, t_{PLH}$		5	—	220	440	ns	
		10	—	100	200		
		15	—	70	140		
Output Transition Time $t_{THL}, t_{TLH}$		5	—	100	200		
		10	—	50	100		
		15	—	40	80		
Minimum Setup Time: $t_s$ D0, D3, SR <sub>IN</sub> , SL <sub>IN</sub> to Clock		5	—	80	160		
		10	—	35	70		
		15	—	20	50		
SELECT 0, SELECT 1 to Clock		5	—	200	400		
		10	—	110	220		
		15	—	65	130		
Minimum Hold Time: $t_H$ D0, D3, SR <sub>IN</sub> , SL <sub>IN</sub> to Clock		5	—	-65	0		
		10	—	-25	0		
		15	—	-15	0		
SELECT 0, SELECT 1 to Clock		5	—	-170	0		
		10	—	-95	0		
		15	—	-55	0		
Minimum Clock Pulse Width $t_W$		5	—	90	180		
		10	—	40	80		
		15	—	25	50		
Maximum Clock Input Frequency $f_{CL}$		5	3	6	—	MHz	
		10	6	12	—		
		15	8	15	—		
Maximum Clock Rise or Fall Time $t_{rCL}, t_{fCL}$		5	—	—	1000	$\mu\text{s}$	
		10	—	—	100		
		15	—	—	100		
Minimum Reset Pulse Width* $t_{WR}$		5	—	150	300	ns	
		10	—	100	200		
		15	—	70	140		
Reset Propagation Delay $t_{PRHL}$		5	—	230	460		
		10	—	90	180		
		15	—	65	130		
Input Capacitance $C_{IN}$	Any Input		—	5	7.5		pF

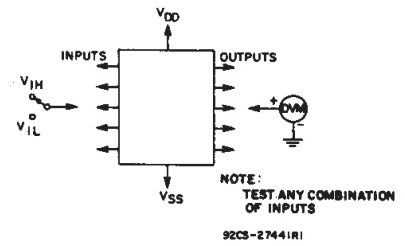


Fig. 12—Input-voltage test circuit.

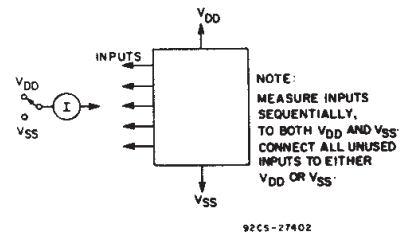
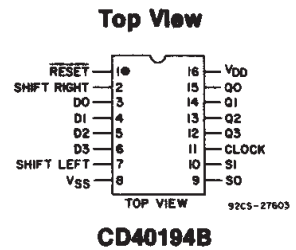


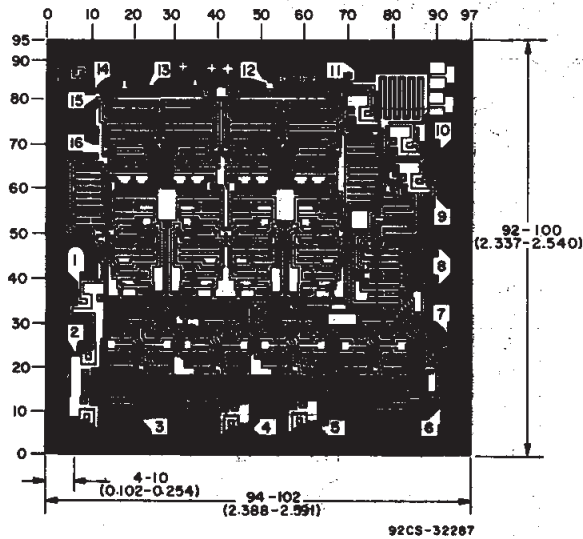
Fig. 13—Input current test circuit.

## TERMINAL DIAGRAM



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## CD40194B Types



*Dimensions and pad layout for CD40194BH*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

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