CD54/74HC195

Data sheet acquired from Harris Semiconductor
SCHS165A

September 1997 - Revised May 2000

High Speed CMOS Logic 4-Bit Parallel Access Register

Features

- **Asynchronous Master Reset**
- **J, $\overline{K}$, (D) Inputs to First Stage**
- **Fully Synchronous Serial or Parallel Data Transfer**
- **Shift Right and Parallel Load Capability**
- **Complementary Output From Last Stage**
- **Buffered Inputs**
- **Typical f_{MAX} = 50MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25^oC**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V**

Description

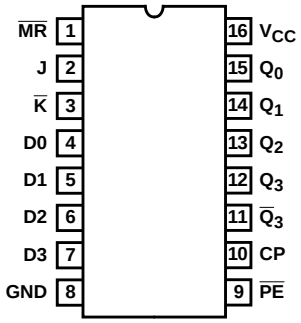
The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The two modes of operation, shift right (Q_0-Q_1) and parallel load, are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is high, and is shifted one bit in the direction Q_0-Q_1-Q_2-Q_3 following each Low to High clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK-type input for special applications and by tying the two pins together, the simple D-type input for general applications. The device appears as four common-clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low to High clock transition, data on the parallel inputs (D0-D3) is transferred to the respective Q_0-Q_3 outputs. Shift left operation (Q_3-Q_2) can be achieved by tying the Q_n outputs to the Dn-1 inputs and holding the $\overline{PE}$ input low.

All parallel and serial data transfers are synchronous, occurring after each Low to High clock transition. The 'HC195 series utilizes edge triggering; therefore, there is no restriction on the activity of the J, $\overline{K}$, Pn and $\overline{PE}$ inputs for logic operations, other than set-up and hold time requirements. A Low on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs Low, independent of any other input condition.

Pinout

CD54HC195
(CERDIP)
CD74HC195
(PDIP, SOIC)
TOP VIEW



Ordering Information

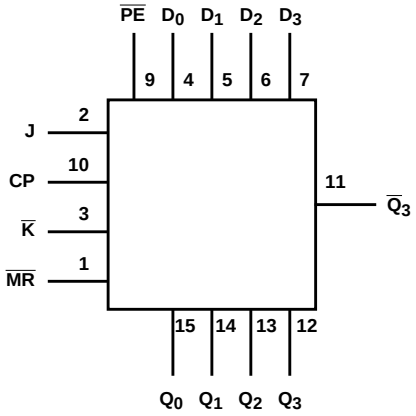
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC195F3A	-55 to 125	16 Ld CERDIP
CD74HC195E	-55 to 125	16 Ld PDIP
CD74HC195M	-55 to 125	16 Ld SOIC

NOTES:

1. When ordering, use the entire part number.
2. Die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

OPERATING MODES	INPUTS						OUTPUT				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	Dn	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	dn	d_0	d_1	d_2	d3	$\overline{d2}$

NOTE: H = High Voltage Level
L = Low Voltage Level,
X = Don't Care
↑ = Transition from Low to High Level
l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition
h = Low Voltage Level One Set-up Time prior to the High to Low Clock Transition,
dn (q_n) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low to High Clock Transition.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 190
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current (Note)	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Prerequisite For Switching Function

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
Clock Frequency	f_{MAX}	-	2	6	-	5	-	4	-	MHz
			4.5	30	-	25	-	20	-	MHz
			6	35	-	29	-	23	-	MHz
$\overline{MR}$ Pulse Width	t_W	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Clock Pulse Width	t_W	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Set-up Time J, $\overline{K}$, $\overline{PE}$ to Clock	t_{SU}	-	2	100	-	125	-	150	-	ns
			4.5	20	-	25	-	30	-	ns
			6	17	-	21	-	26	-	ns
Hold Time J, $\overline{K}$, $\overline{PE}$ to Clock	t_H	-	2	3	-	3	-	3	-	ns
			4.5	3	-	3	-	3	-	ns
			6	5	-	3	-	3	-	ns
Removal Time, $\overline{MR}$ to Clock	t_{REM}	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, CP to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
Propagation Delay, $\overline{MR}$ toOutput	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
Output Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF
CP to Q_n Propagation Delay	t_{PLH}, t_{PHL}	C_L = 15pF	5	14	-	-	-	ns
$\overline{MR}$ to Q_n	t_{PHL}	C_L = 15pF	5	13	-	-	-	ns
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5	50	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	C_L = 15pF		45	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per flip-flop.
5. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveforms

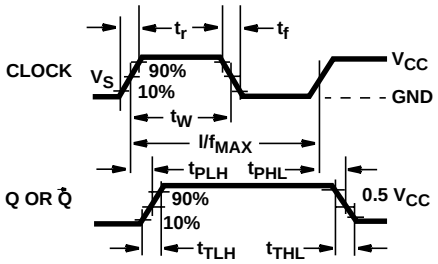


FIGURE 1. CLOCK PRE-REQUISITE AND PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES

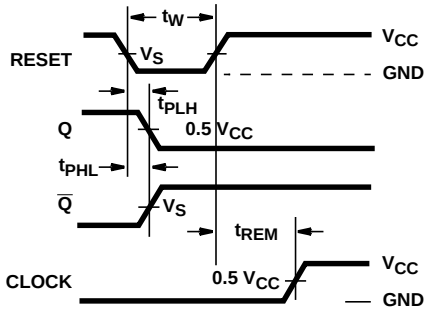


FIGURE 2. MASTER RESET PRE-REQUISITE AND PROPAGATION DELAYS

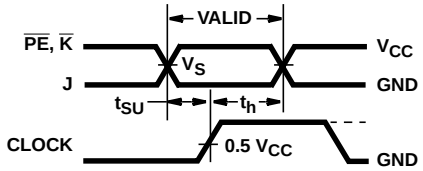


FIGURE 3. J, $\overline{K}$ OR PARALLEL ENABLE PRE-REQUISITE TIMES

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