TEXAS INSTRUMENTS

CY29FCT818T

SCCS012 - May 1994 - Revised February 2000

Diagnostic Scan Register

Features

- **Function, pinout and drive compatible with FCT, F Logic and AM29818**
- **FCT-C speed at 6.0 ns max. (Com'l), FCT-A speed at 12.0 ns max. (Mil)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 20 mA (Mil)**
  Source current 32 mA (Com'l), 3 mA (Mil)
- **8-Bit pipeline and shadow register**
- **ESD > 2000V**

Functional Description

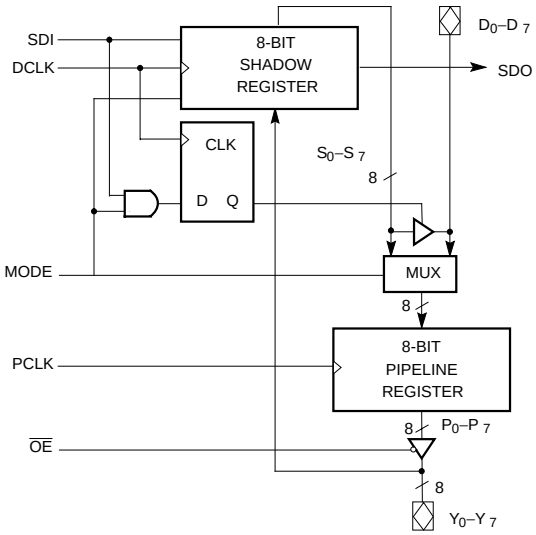
The FCT818T contains a high-speed 8-bit general-purpose data pipeline register and a high-speed 8-bit shadow register. The general-purpose register can be used in an 8-bit wide data path for a normal system application. The shadow register is designed for applications, such as diagnostics in sequential circuits, where it is desirable to load known data at a specific location in the circuit and to read the data at that location.

The shadow registers can load data from the output of the FCT818T, and can be used as a right-shift register with bit-serial input SDI and output SDO, using DCLK. The data register input is multiplexed to enable loading from the shadow register or from the data input pins using PCLK. Note that data can be loaded simultaneously from the shadow register to the pipeline register, and from the pipeline register to the shadow register provided set-up and hold time requirements are satisfied with respect to the two independent clock inputs.

In a typical application, the general-purpose register in the FCT818T replaces an 8-bit data register in the normal data path of a system. The shadow register is placed in an auxiliary bit-serial loop which is used for diagnostics. During diagnostic operation, data is shifted serially into the shadow register, then transferred to the general purpose register to load a known value into the data path. To read the contents at that point in the data path, the data is transferred from the data register into the shadow register, then shifted serially in the auxiliary diagnostic loop to make it accessible to the diagnostics controller. This data is then compared with the expected value to diagnose faulty operation of the sequential circuit.

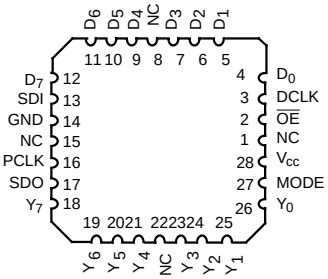
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

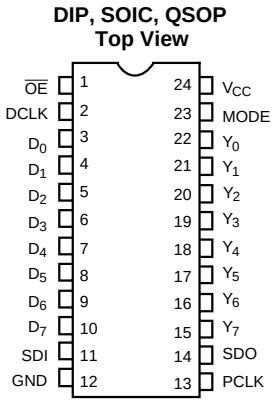


Pin Configurations

LCC
Top View



DIP, SOIC, QSOP
Top View



Function Table[1]

Inputs			Inputs		Shadow Register	Pipeline Register	Operation
MODE	SDI	DCLK	PCLK	SDO			
L	X	⌐	X	S_7	$S_0 \leftarrow SDI$ $S_i \leftarrow S_{i-1}$	NA	Serial Shift; D_7–D_0 Output Disabled
L	X	X	⌐	S_7	NA	$P_i \leftarrow D_i$	Load Pipeline Register from Data Input
H	L	⌐	X	L	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y Output
H	H	⌐	X	H	Hold	NA	Hold Shadow Register; D_7–D_0 Output Enabled
H	X	X	⌐	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied .....–65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation 0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	All	–40°C to +85°C	5V ± 5%
Military[4]	All	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=–15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=–3 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=20 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT}=0.5V				–10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit

Notes:

1. NA = Not Applicable
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[8]

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Document #: 38-00275-B

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V, f_1=0, Outputs Open [8]	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Input Toggling, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V		0.25	mA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V		5.3	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND		7.3	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, Eight Bits and Four Controls Toggling, f_1=5 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V		17.8[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, Eight Bits and Four Controls Toggling, f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND		30.8[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[12]

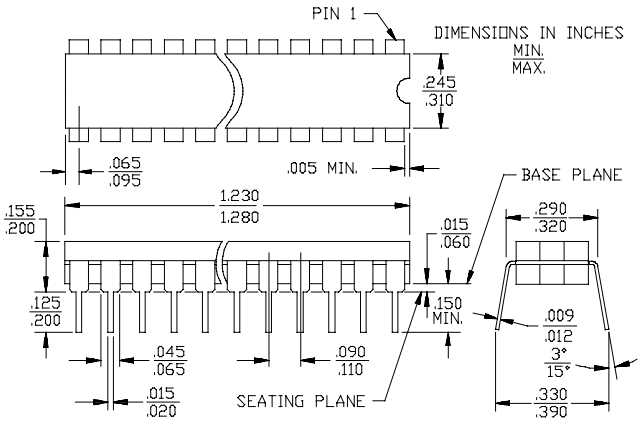
Parameter	Description	FCT818AT Military		FCT818CT Commercial		Unit	Fig. No.[13]
		Min.	Max.	Min.	Max.		
t_{PD}	Propagation Delay						
	PCLK to Y		12		6.0	ns	5
	MODE to SDO		18		7.2	ns	6
	SDI to SDO		18		7.1	ns	3
	DCLK to SDO		30		7.2	ns	5
t_S	Set-Up Time						
	D to PCLK	6		2.0		ns	
	MODE to PCLK	15		3.5		ns	
	Y to DCLK	5		2.0		ns	
	MODE to DCLK	12		3.5		ns	4
	SDI to DCLK	10		3.5		ns	
	DCLK to PCLK	15		3.5		ns	
	PCLK to DCLK	45		8.5		ns	
t_H	Hold Time						
	D to PCLK	2		1.5		ns	
	MODE to PCLK	0		0		ns	
	Y to DCLK	5		1.5		ns	4
	MODE to DCLK	5		1.5		ns	
	SDI to DCLK	0		0		ns	
t_{PLZ}	Output Disable Time LOW						
	$\overline{OE}$ to Y		20		5.5	ns	7
	DCLK to D		45		5.5	ns	5
t_{PHZ}	Output Disable Time HIGH						
	$\overline{OE}$ to Y		30		8.0	ns	8
	DCLK to D		90		8.0	ns	5
t_{PZL}	Output Enable Time LOW						
	$\overline{OE}$ to Y		20		8.0	ns	7
	DCLK to D		35		9.0	ns	5
t_{PZH}	Output Enable Time HIGH						
	$\overline{OE}$ to Y		20		8.5	ns	8
	DCLK to D		30		9.0	ns	5
t_W	Pulse Width						
	PCLK (HIGH and LOW)	15		5.0		ns	5
	DCLK (HIGH and LOW)	25		5.0		ns	5

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY29FCT818CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818CTQCT	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
12.0	CY29FCT818ATDMB	D14	24-Lead (300-Mil) CerDIP	Military

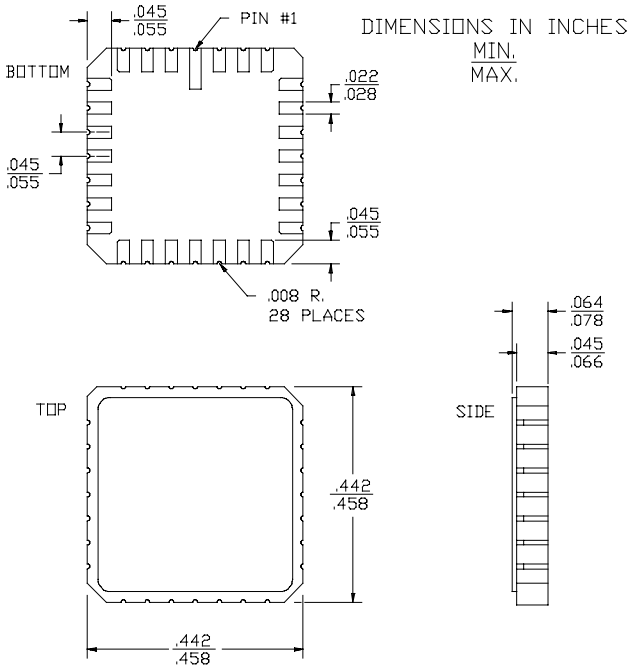
Notes:
12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.

Package Diagrams

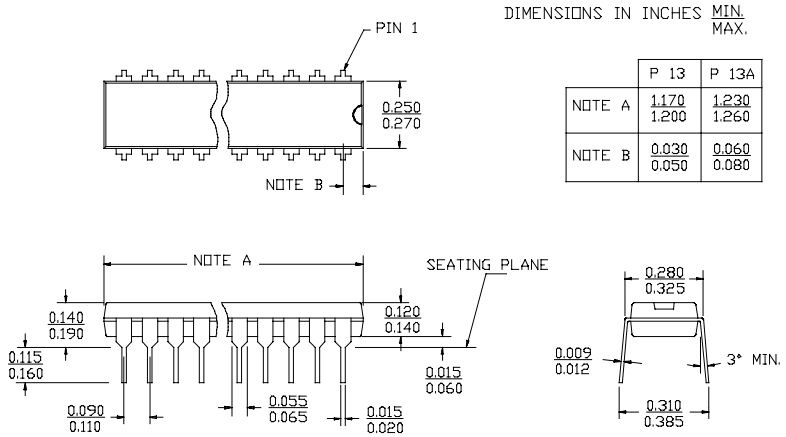
24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D-9 Config.A



28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4



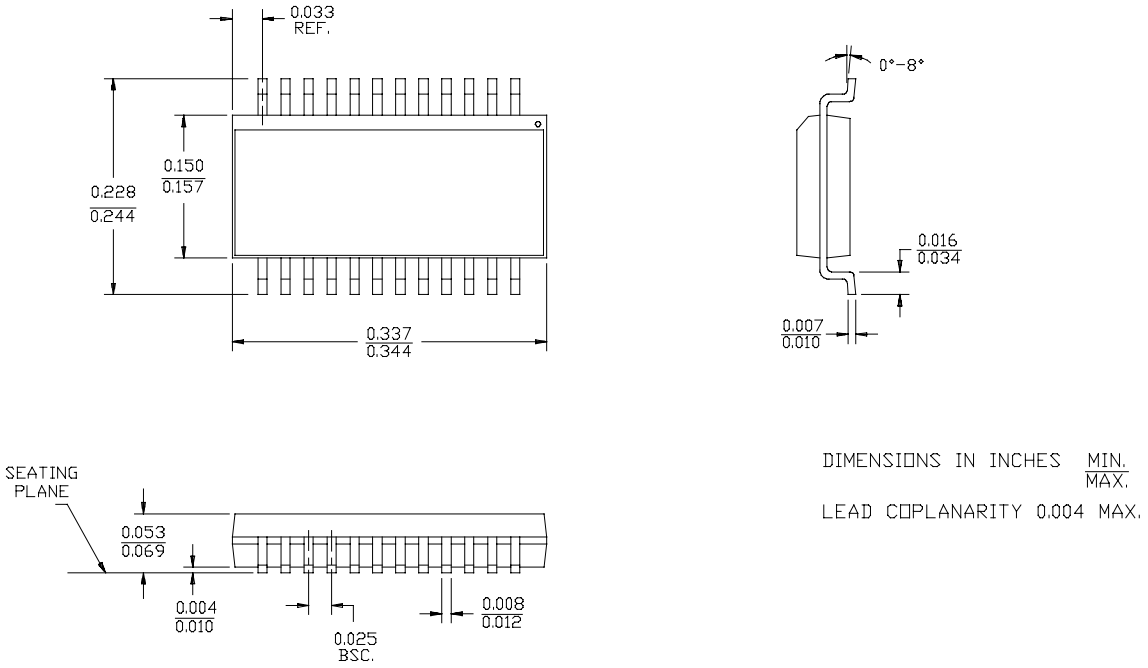
24-Lead (300-Mil) Molded DIP P13/P13A



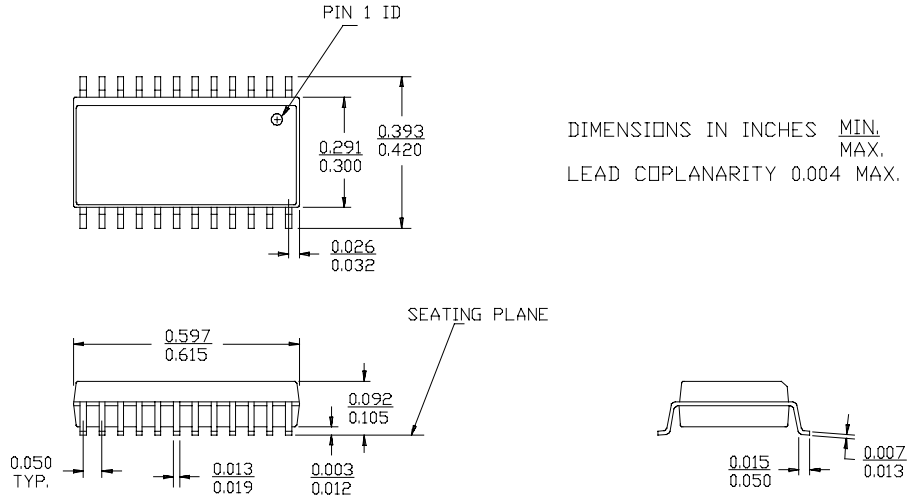
	P 13	P 13A
NOTE A	1.170 / 1.200	1.230 / 1.260
NOTE B	0.030 / 0.050	0.060 / 0.080

Package Diagrams (continued)

24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.